Combination of Ultra-Thin High-Density Silicon Capacitors and Fan-out Packaging Glass Substrate

Abstract

This innovation describes the combination of Ultra-Thin High-Density Silicon Capacitors (UTHDSCs) with fan-out packaging glass substrates, aimed at enhancing electrical performance in advanced semiconductor applications. The innovation focuses on improving current density, capacitance density, signal integrity, and thermal management within the packaging structure. By embedding UTHDSCs within or near the Redistribution Layer (RDL) of fan-out packaging glass substrates, this technology optimizes power distribution and reduces parasitic inductance, making it suitable for high-frequency and high-power electronics. The innovation also addresses the challenges associated with the mechanical fragility of fan-out packaging glass substrates, providing enhanced reliability of the packaging structure. Furthermore, innovations in through-hole and interconnect designs are introduced to support efficient electrical pathways between UTHDSCs and other components within the package. These improvements enable more robust, high-performance semiconductor packaging solutions for applications in 5G, automotive, aerospace, and power electronics. The integration of UTHDSCs into fan-out packaging glass substrates represents a novel approach that significantly improves electrical and thermal performance, marking a key advancement in semiconductor packaging technology.

[Designated representative picture] Figure 1.

[A brief explanation of the symbols of the representative diagram]

1. Fan-out packaging glass substrate
2. Redistribution Layer
3. Ultra-thin high-density silicon capacitor
4. Interconnection channels
5. Chip
6. Solder ball
13. Other components
16. Encapsulation protective layer

Combination of Ultra-Thin High-Density Silicon Capacitors and Fan-out Packaging Glass Substrate

Specification

【Technical field】

[0001] This new type relates to semiconductor packaging technology, especially about combining ultra-thin high-density silicon capacitors (UTHDSCs) with glass substrates in fan-out packaging (Fan-Out Wafer-Level Packaging, FOWLP) technology to increase current density and capacitance density. , thermal management performance and signal integrity. This technology is suitable for high-performance electronic devices, such as 5G communications, high-frequency applications, automotive electronics and high-power processing systems.

【Prior technology】

[0002] Traditional fan-out packaging technology usually uses organic substrates or silicon substrates for signal redistribution and packaging. Although it has made significant progress in high-frequency signal processing and efficient power management, it has insufficient current density, capacitance density and Problems such as limited thermal management effect. In addition, substrates based on organic materials have certain limitations in terms of thermal stability and electrical performance. The use of ultra-thin high-density silicon capacitors has mainly focused on increasing capacitance density in the past, but has not been fully applied to the glass substrate structure of fan-out packages.

【New content】

[0003] The present invention proposes a method of combining an ultra-thin high-density silicon capacitor with a fan-out packaging glass substrate. By directly embedding the ultra-thin high-density silicon capacitor in or adjacent to a redistribution layer (RDL), the current density and capacitance density are significantly improved, and the parasitic inductance is reduced. The fan-

out packaging glass substrate has excellent insulation and thermal conductivity properties, making the overall packaging structure more stable when processing high-power and high-frequency signals. This technology also solves the problems of mechanical strength and thermal management of fan-out packaging glass substrates, enhancing the mechanical stability and reliability of the overall package.

【Simple explanation of the diagram】

[0004]
[Figure 1]: A cross-sectional structural diagram of the present invention.

[Figure 2]: Shows a detailed view of the redistribution layer (RDL) on the glass substrate, describing how electrical signals pass through the UTHDSCs to enhance current density and optimize power delivery.

[Figure 3]: Shows an enlarged view of a portion of the UTHDSCs and interconnect channel, highlighting its detailed design, illustrating the signal connection between the capacitor and other components and the mechanism for reducing parasitic effects.

[Figure 4]: Schematic showing thermal management optimization, illustrating how UTHDSCs integration improves the heat dissipation capabilities of the overall package structure, especially on glass substrates.

[Figure 5]: A graph showing the mechanical stress test results, illustrating the stability of UTHDSCs under thermal cycling and mechanical deformation conditions, ensuring the long-term reliability of the packaging structure.

【Implementation】

[0005] Please refer to FIG. 1, FIG. 2, FIG. 3 and FIG. 4. First, the fan-out packaging glass substrate 1 is pre-processed to prepare as a base material for the fan-out packaging. The fan-out packaging glass substrate 1 has high thermal conductivity and insulation performance, ensuring good temperature control and signal stability under high power applications. Then, through advanced manufacturing technology, a redistribution layer 2 composed of multiple layers of metal wires and dielectric layers is constructed on the fan-out packaging glass substrate 1 to form a highly dense and low-loss signal

path and current transmission network. Afterwards, using high-precision process technology, the ultra-thin high-density silicon capacitor 3 is precisely embedded or arranged in the redistribution layer 2. The capacitor, with its high capacitance and low equivalent series resistance (ESR) characteristics, greatly improves the current density and power management capabilities of the packaging structure. By enhancing the current density 7 and optimizing power transfer 8, the top electrode 9 and the bottom electrode 10 of the capacitor are respectively connected to other components 13 through the interconnection channel 4, forming an efficient electrical interconnection to ensure efficient current transfer and capacitance enhancement, reduce parasitic effects and enhance signal integrity. The chip 5 is arranged on the upper layer of the packaging structure, and is closely combined with the redistribution layer 2 and the ultra-thin high-density silicon capacitor 3 to ensure power management and data transmission efficiency. The overall structure is further added with a packaging protection layer 16 to enhance its durability and environmental protection performance. The completed packaging structure can effectively improve electrical performance and reduce losses caused by parasitic effects. The heat management mechanism in the overall packaging structure, the fan-out packaging glass substrate 1 acts as a highly efficient heat dissipation material, which quickly directs the heat flow 14 generated by the chip 5 and the ultra-thin high-density silicon capacitor 3 to the heat sink 15 below. This thermal management design significantly improves the heat dissipation efficiency of the package structure, ensuring that electronic devices maintain stability and reliability under high power operation.

【Explanation of symbols】

[0006]

1. Fan-out packaging glass substrate
2. Redistribution Layer
3. Ultra-thin high-density silicon capacitors
4. Interconnection channels
5. Chip
6. Solder ball
7. Enhance current density
8. Optimize power delivery
9. Top electrode
10. Bottom electrode

11. Parasitic capacitance
12. Insulating layer
13. Other components
14. Heat flow
15. Heat sink
16. Encapsulation protective layer
17. Thermal Cycling (-40 ℃ to 125 ℃)
18. Mechanical deformation
19. Control Group
20. Package structure

Combination of Ultra-Thin High-Density Silicon Capacitors and Fan-out Packaging Glass Substrate

Claims

[Claim 1] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate, wherein:

A fan-out packaging glass substrate having an upper surface and a lower surface;

An ultra-thin high-density silicon capacitor (UTHDSCs), which uses a high aspect ratio deep trench structure to increase capacitance density and is ultra-thinned through silicon vias (TSV) or thin film stacking technology to further reduce package height and parasitic parameters. The capacitor is embedded in the redistribution layer. The electrodes of the silicon capacitor are directly connected to the interconnect channels in the redistribution layer to increase current density and reduce parasitic effects;

A redistribution layer (RDL), which covers the entire upper surface of the fan-out package glass substrate and contains at least one layer of metal wire and dielectric layer for signal redistribution and current transmission;

A package structure comprising at least one chip and multiple redistribution layers (RDL), wherein the chip is electrically connected to the RDL through solder balls, microbumps or through silicon vias (TSV), and each RDL is composed of metal wires and dielectric layers to support high-density signal paths and power transmission;

A packaging protection layer is disposed outside the packaging structure and is used to cover the fan-out packaging glass substrate, the redistribution layer (RDL) and the embedded ultra-thin high-density silicon capacitors (UTHDSCs) to provide an environmental barrier and structural protection.

[Claim 2] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the fan-out packaging glass substrate has high thermal conductivity and excellent insulation properties, and is used to enhance the heat dissipation capacity and electrical performance of the packaging structure.

[Claim 3] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the packaging structure comprises a plurality of redistribution layers (RDL), each layer consisting of a metal conductor and a dielectric layer, to support high-density signal paths and power transfer.

[Claim 4] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the packaging structure further comprises a packaging protection layer for covering the fan-out packaging glass substrate, the redistribution layer and the embedded ultra-thin high-density silicon capacitors (UTHDSCs) to provide an environmental barrier and structural protection.

[Claim 5] A combination of an ultra-thin high density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the capacitance of the embedded ultra-thin high density silicon capacitor (UTHDSCs) is not less than 0.1 microfarad per square millimeter, and is used for stable power management in high-performance electronic devices.

[Claim 6] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the ultra-thin high-density silicon capacitor (UTHDSCs) is embedded in a redistribution layer above the fan-out packaging glass substrate to increase capacitance density, reduce parasitic inductance, and improve signal integrity and thermal management.

[Claim 7] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the redistribution layer (RDL) comprises multiple metal layers and electrical interconnect channels to ensure efficient current transmission between the ultra-thin high-density silicon capacitor (UTHDSCs) and other packaging components.

[Claim 8] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the thermal management system comprises a layer of thermally conductive material to optimize heat distribution in the package, particularly in high-power applications, to enhance the stability of the package.

[Claim 9] A combination of an ultra-thin high density silicon capacitor and a fan-out packaging glass substrate according to any one of Claim 1 to 8, wherein the fan-out packaging glass substrate may be selected to include variations of different materials, including but not limited to glass, ceramics, organic materials or high thermal conductivity polymers, and ultra-thin high density silicon capacitors (UTHDSCs) may be combined with fan-out packaging substrates of these different materials to enhance their performance and application flexibility under different environmental conditions.

[Claim 10] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the packaging structure is suitable for high-frequency electronic devices, such as 5G communication systems, automotive electronic devices, and high-power processors.

[Claim 11] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the packaging structure is applied to a 5G communication system, and the ultra-thin high-density silicon capacitor (UTHDSCs) provides high-frequency signal stability and power management, can effectively reduce parasitic effects and improve the signal integrity and power transfer efficiency of the system, and is suitable for 5G base stations, user-end equipment, and high-frequency network equipment.

[Claim 12] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the packaging structure is applied to automotive electronic devices, and the ultra-thin high-density silicon capacitors (UTHDSCs) are combined with automotive electronic control units (ECUs) or autonomous driving systems to provide stable power management and excellent thermal management performance, capable of coping with high vibration, high temperature and changing vehicle environments.

[Claim 13] A combination of an ultra-thin high-density silicon capacitor and a fan-out packaging glass substrate according to Claim 1, wherein the packaging structure is applied to a high-performance processor, and the ultra-thin high-density silicon capacitor (UTHDSCs) can be combined in the processor package to increase the capacitance density, reduce power loss and

improve the heat dissipation performance of the processor when it operates efficiently, and is suitable for use in servers, AI accelerators, high-performance computing and other fields.

Combination of Ultra-Thin High-Density Silicon Capacitors and Fan-out Packaging Glass Substrate

Figures

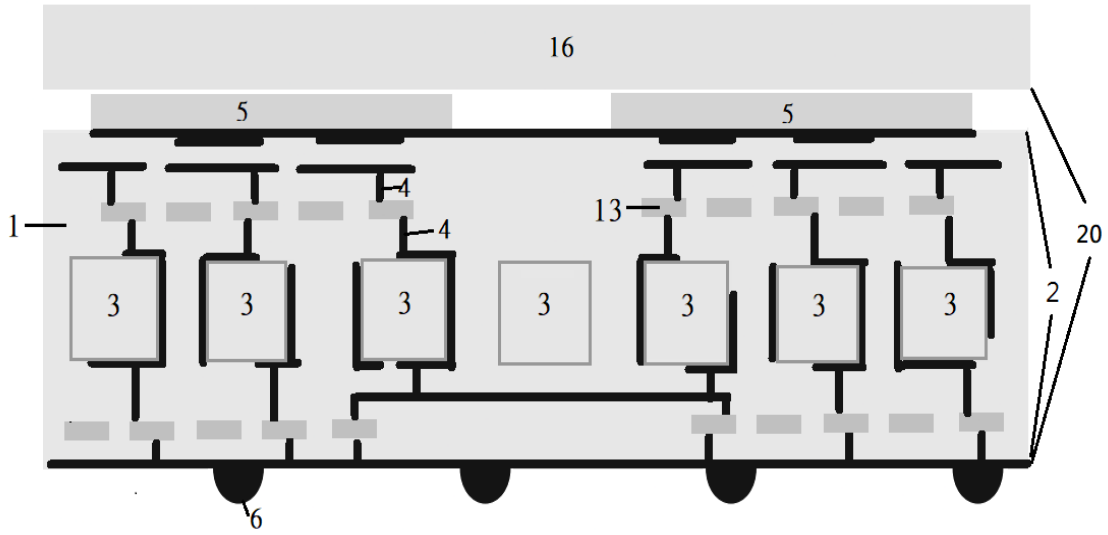

Figure 1

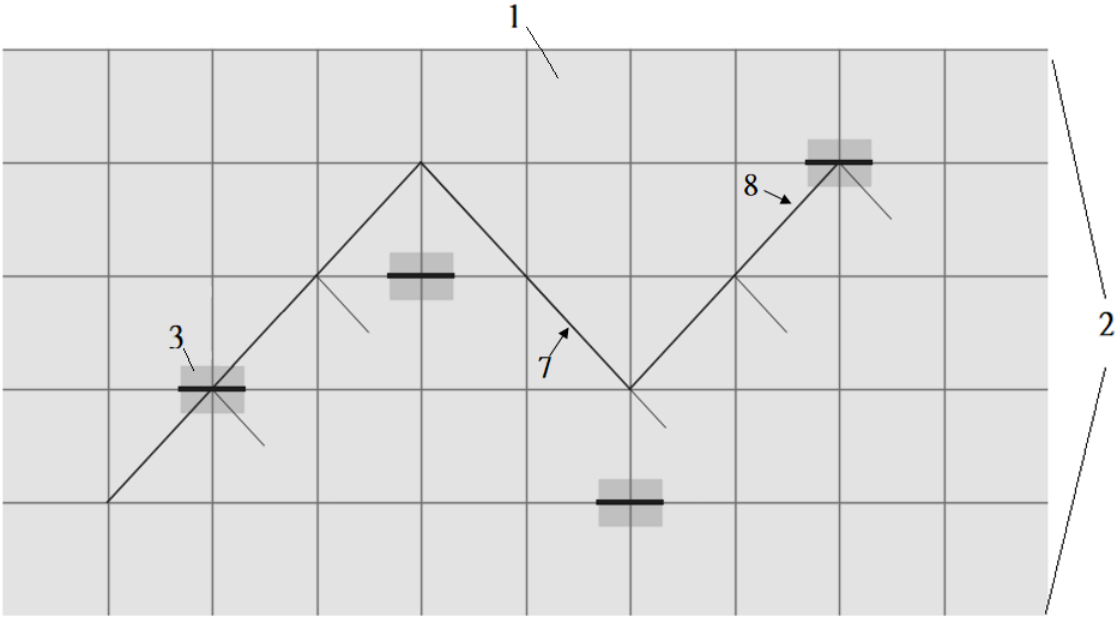

Figure 2

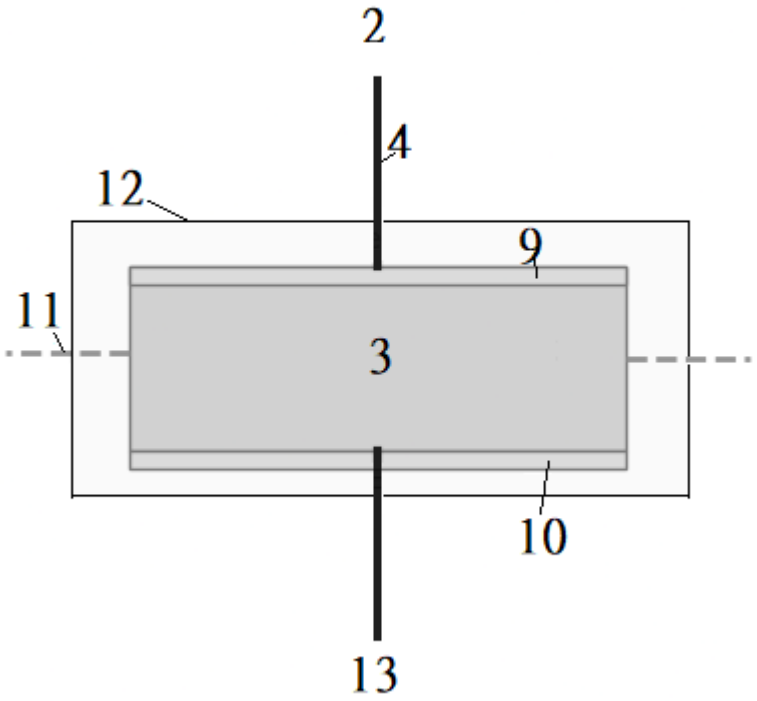

Figure 3

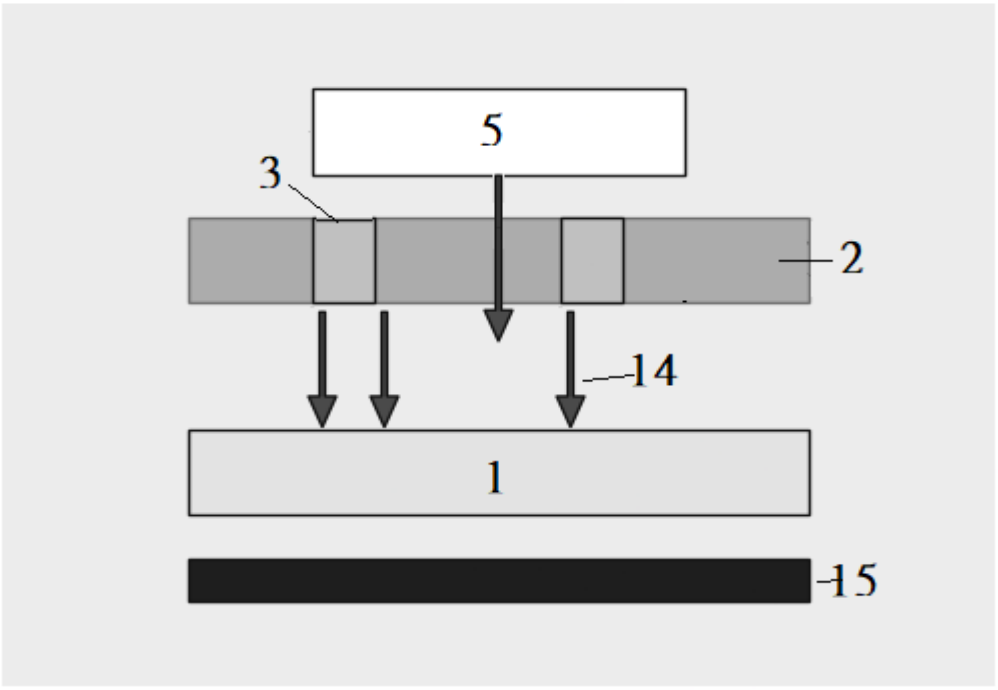

Figure 4

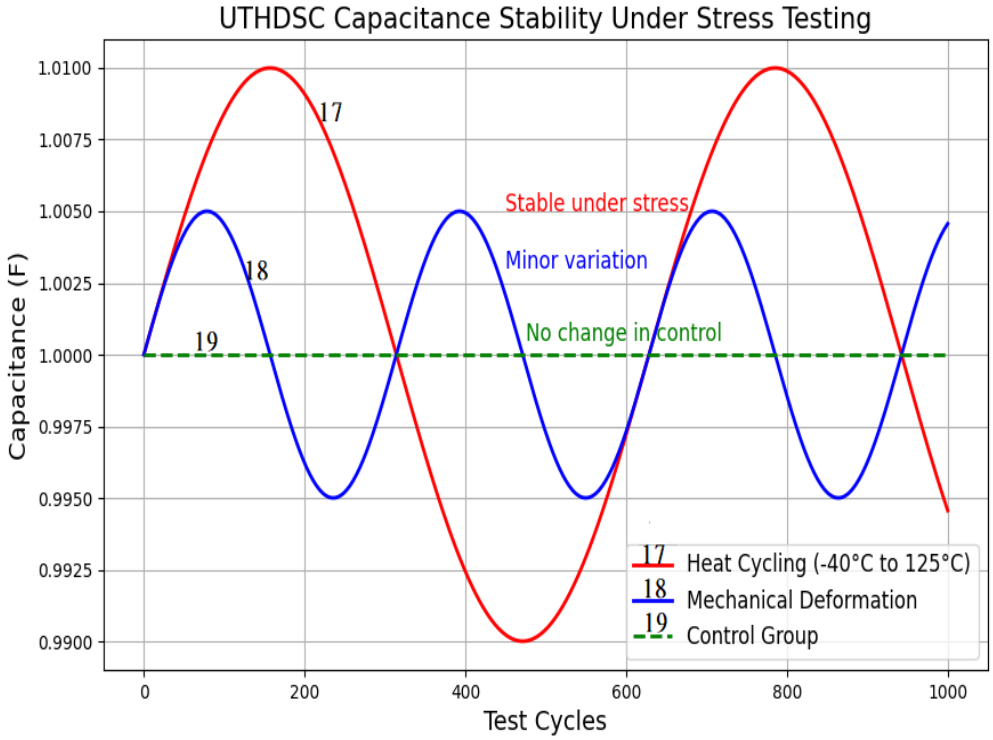
UTHDSC Capacitance Stability Under Stress Testing
Capacitance (F)
Test Cycles
1.0100
1.0075
1.0050
1.0025
1.0000
0.9975
0.9950
0.9925
0.9900
0
200
400
600
800
1000
17
18
19
Stable under stress
Minor variation
No change in control
17 Heat Cycling (-40°C to 125°C)
18 Mechanical Deformation
19 Control Group

Figure 5