Combination of ultra-thin high-density silicon capacitors and power supply network (BSPDN) on the backside of 2nm process

Abstract

The new type relates to a combination of ultra-thin high-density silicon capacitors (UTHDSC) suitable for 2-nanometer manufacturing processes, especially for backside power supply networks (BSPDN). The 2nm node introduces higher transistor density and faster switching speeds, leading to significant power supply noise that can compromise signal integrity and device stability. The UTHDSCs in this utility model effectively suppress high-frequency noise through high capacitance density and low Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), while maintaining stable voltage supply. Additionally, UTHDSCs are optimized for leakage current mitigation, using advanced dielectric materials to reduce leakage under high-temperature operation, ensuring low power loss and high efficiency. UTHDSCs are embedded in BSPDN to improve power delivery proximity, enhancing efficiency in high-density chip systems and reducing power fluctuations. This technology is particularly suitable for high-performance computing (HPC), artificial intelligence (AI) processors, and mobile devices, providing a reliable power delivery system in smaller node technologies. The new model also introduces a combination suitable for wafer-level fan-out packaging (WLFO), ensuring that UTHDSC can achieve high-performance packaging integration without increasing the equipment volume.

[Designated Representative Figure]
Figure 1: Cross-sectional View of UTHDSCs Integrated within a 2nm Node Device Using BSPDN Architecture

[A brief explanation of the symbols of the representative diagram]
1. Wafer
2. BSPDN
3. UTHDSC

4. Metal Interconnect Layer
5. Transistor Layer
10. Insulation Layer
17. Dielectric layer

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Specifications

【Technical field】

[0001] This new type involves ultra-thin high-density silicon capacitor (UTHDSC) technology, especially for application combinations in semiconductor devices. It is suitable for power stability and signal integrity management of 2nm process and backside power supply network (BSPDN) architecture. This new technology focuses on noise suppression, leakage current reduction, and power efficiency optimization in high-density, fast-switching circuits.

【Prior technology】

[0002] With the advancement of semiconductor process technology, node size has shrunk to 2 nanometers, and transistor density and speed have increased significantly. However, these advances also bring corresponding challenges, including power supply noise issues and increased leakage current under high-temperature operation. Existing capacitor technology is difficult to meet these needs. The size and performance of traditional capacitors cannot effectively adapt to the high capacitance density and low resistance characteristics required in advanced processes. Especially in the backside power supply network (BSPDN) architecture, the performance of the capacitor plays a key role in the stability of the overall power supply, but the existing technology lacks effective solutions.

【New content】

[0003] This new model proposes an ultra-thin high-density silicon capacitor (UTHDSC) suitable for the 2-nanometer process, specifically designed for the backside power supply network (BSPDN). The silicon capacitor has high capacitance density and low equivalent series resistance (ESR) and low equivalent series inductance (ESL), which can effectively suppress high-frequency noise and provide stable voltage supply. In addition, the UTHDSC in this new model uses advanced dielectric materials to maintain low leakage current in high temperature environments, ensuring energy saving and efficient operation. This novel also introduces a combination of integration technologies suitable for wafer-level packaging (WLFO), allowing for high-efficiency packaging without increasing device volume.

[Simple explanation of the diagram]

【0004】

[Figure 1]: Cross-sectional view of ultra-thin high-density silicon capacitor (UTHDSC) package

[Figure 2]: Schematic diagram of UTHDSC suppressing power supply noise in high-frequency circuits, showing a comparison of noise waveforms when used with or without capacitors.

[Figure 3]: Schematic diagram of the manufacturing process of UTHDSC, showing the manufacturing steps and stacking process of its ultra-thin structure.

[Figure 4]: Comparison of leakage current levels between UTHDSC and traditional capacitors in the 2nm process.

[Figure 5]: Performance analysis diagram of UTHDSC noise reduction in backside power supply network (BSPDN).

[Figure 6]: Thermal performance of UTHDSC in 2nm node, demonstrating its stability at different operating temperatures properties and low leakage current.

[Figure 7]: Implementation.

【Implementation】

【0005】Referring to Figures 1 and 7, this new model provides UTHDSC3 using multi-layer dielectric materials 9 and a high-density stacking structure. First, an ultra-thin dielectric layer 17 is deposited on the wafer 1. This material has extremely high breakdown voltage and excellent thermal stability, ensuring reliability under the 2-nanometer process. Then, through advanced micro-processing technology, silicon layers 18 and dielectric layers 17 are alternately stacked to form a structure with high capacitance density. This ultra-thin layer is only a few nanometers thick, allowing higher capacitance to be achieved within a limited die area. UTHDSC3 is embedded in the Backside Power Delivery Network (BSPDN)2 via a Wafer Level Fan-Out Package (WLFO)8. In this embodiment, UTHDSC3 is directly embedded in the backside power supply network 2 of the chip and connected to the transistor layer 5 and the metal interconnection layer 4 to reduce parasitic effects in power transmission, such as parasitic inductance and resistance. Such an integration method can not only improve power supply efficiency, but also shorten the power supply path, thereby significantly reducing voltage fluctuations and improving overall stability. In order to further improve power supply stability, UTHDSC3 is

designed to suppress high-frequency noise. Its low equivalent series resistance (ESR)6 and low equivalent series inductance (ESL)7 characteristics ensure that it can respond quickly to voltage changes in ultra-high-speed switching circuits and effectively suppress noise caused by high-speed operation. In the implementation, the UTHDSC3 is placed in the core area of the backside power supply network (BSPDN) 2, so that it can directly affect the power supply of the high-density transistor combination of the transistor layer 5, thereby maintaining signal integrity in high-frequency operation.

In this implementation, UTHDSC3 uses advanced dielectric materials 9 to reduce leakage current in the 2nm process. When working in a high-temperature environment, traditional capacitors are prone to leakage, leading to energy waste. However, by optimizing the material selection and structural design of UTHDSC3, its leakage current can be significantly reduced, maintaining low energy consumption at temperatures up to 85°C, extending the service life of the device and improving overall energy efficiency.

[Explanation of symbols]

【0006】

1.Wafer
2.BSPDN (Backside Power Supply Network)
3.UTHDSC (ultra-thin high-density silicon capacitor)
4.Metal Interconnect Layer
5.Transistor Layer
6.ESR (equivalent series resistance)
7.ESL (equivalent series inductance)
8.WLFO (wafer level fan-out packaging)
9.Dielectric materials
10. Insulation Layer
11. Wafer deposition
12.Printing
13. Etching
14. Dielectric material applications
15. Multi-layer stacking
16. Stacking process to maximize capacitance density
17. Dielectric layer
18. Silicon layer

Claims

[Claim 1] A combination of ultra-thin high-density silicon capacitors and a power supply network on the backside of a 2nm process, including:
Ultra-thin high-density silicon capacitor body: Contains multiple alternately stacked dielectric layers and conductive layers. The material of the dielectric layer is a high dielectric constant material (such as barium titanate or zirconium oxide) to provide more than 100 μF/ mm² capacitance density;
Substrate structure: The ultra-thin high-density silicon capacitor body is embedded in the back power supply network of the substrate structure using wafer-level fan-out packaging (WLFO) technology to reduce parasitic resistance and parasitic inductance;
Conductive interface: provided between the ultra-thin high-density silicon capacitor bodies for high-efficiency power transmission, the conductive interface has an equivalent series resistance (ESR) of less than 0.1 ohm;
Thermal Stable Design: Contains a multi-layer redundant dielectric layer structure that maintains low leakage current of less than 0.01 microamps at operating temperatures up to 150°C;
Integrated structure: The ultra-thin high-density silicon capacitor is directly embedded inside the semiconductor component of the 2nm process to form a compact design, while optimizing the power transmission efficiency and power supply stability of the back power supply network;
Anti-electromagnetic interference function: The ultra-thin high-density silicon capacitor body can actively suppress electromagnetic interference (EMI) and high-frequency noise in the back power supply network, thereby improving signal integrity and ensuring reliable operation.

[Claim 2] The combination of ultra-thin high-density silicon capacitors and a backside power supply network in a 2-nanometer process as described in Claim 1, characterized in that it is used in power management of mobile devices, high-performance computing and artificial intelligence chips, and Provides stable power supply performance under extreme operating conditions.

[Claim Item 3] The combination of ultra-thin high-density silicon capacitors in the back power supply network of the 2nm process as described in Claim 1, is characterized in that it is used in power amplifiers of 5G communication base stations by reducing high-frequency noise and Stable voltage output and enhance the stability of signal transmission.

[Claim 4] The combination of ultra-thin high-density silicon capacitors and a backside power supply network in a 2-nanometer process as described in Claim 1 is characterized by being used in advanced driver assistance systems (ADAS) of autonomous vehicles to provide low leakage , High-stability power supply ensures the reliability of vehicle sensors and computing modules.

[Claim 5] The combination of the ultra-thin high-density silicon capacitor as described in Claim 1 and the power supply network on the back of the 2nm process is characterized by being used in low-power modules of Internet of Things devices to reduce energy in standby states losses while ensuring stable power supply at startup.

[Claim 6] The combination of the ultra-thin high-density silicon capacitor as described in Claim 1 and the back power supply network in a 2-nanometer process is characterized in that it is used in a server power supply system in a high-performance computing data center to improve Improves power supply quality under load fluctuation conditions and reduces the risk of server shutdown.

Figures.

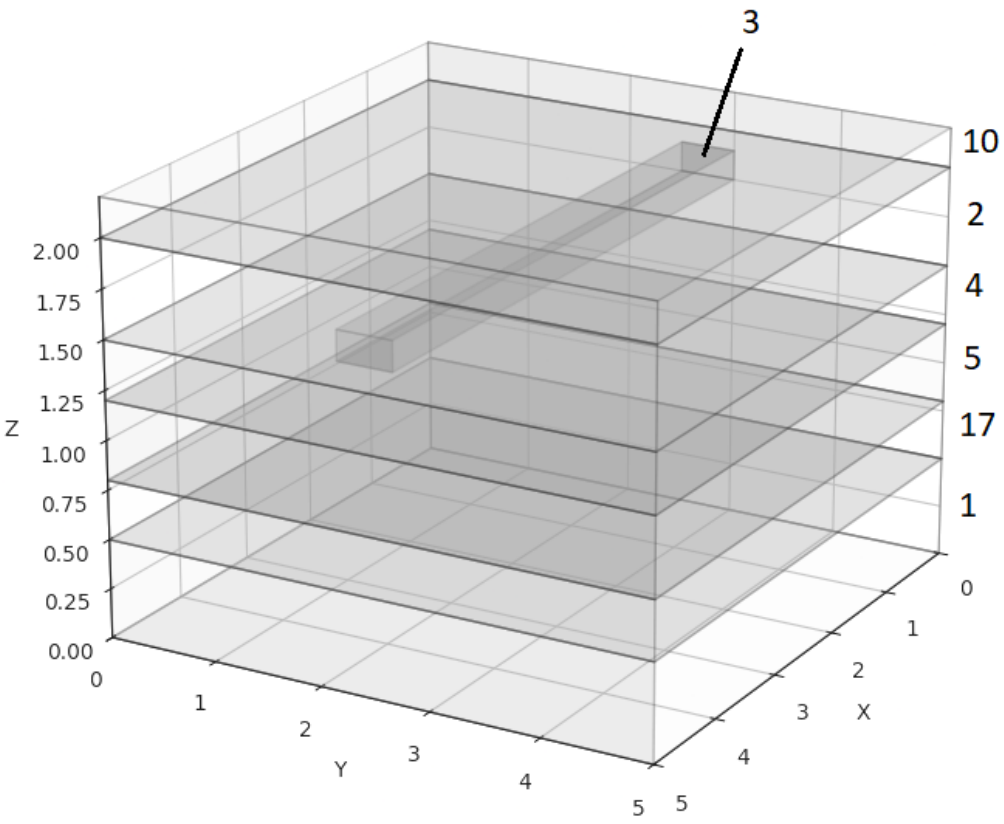

Figure 1.

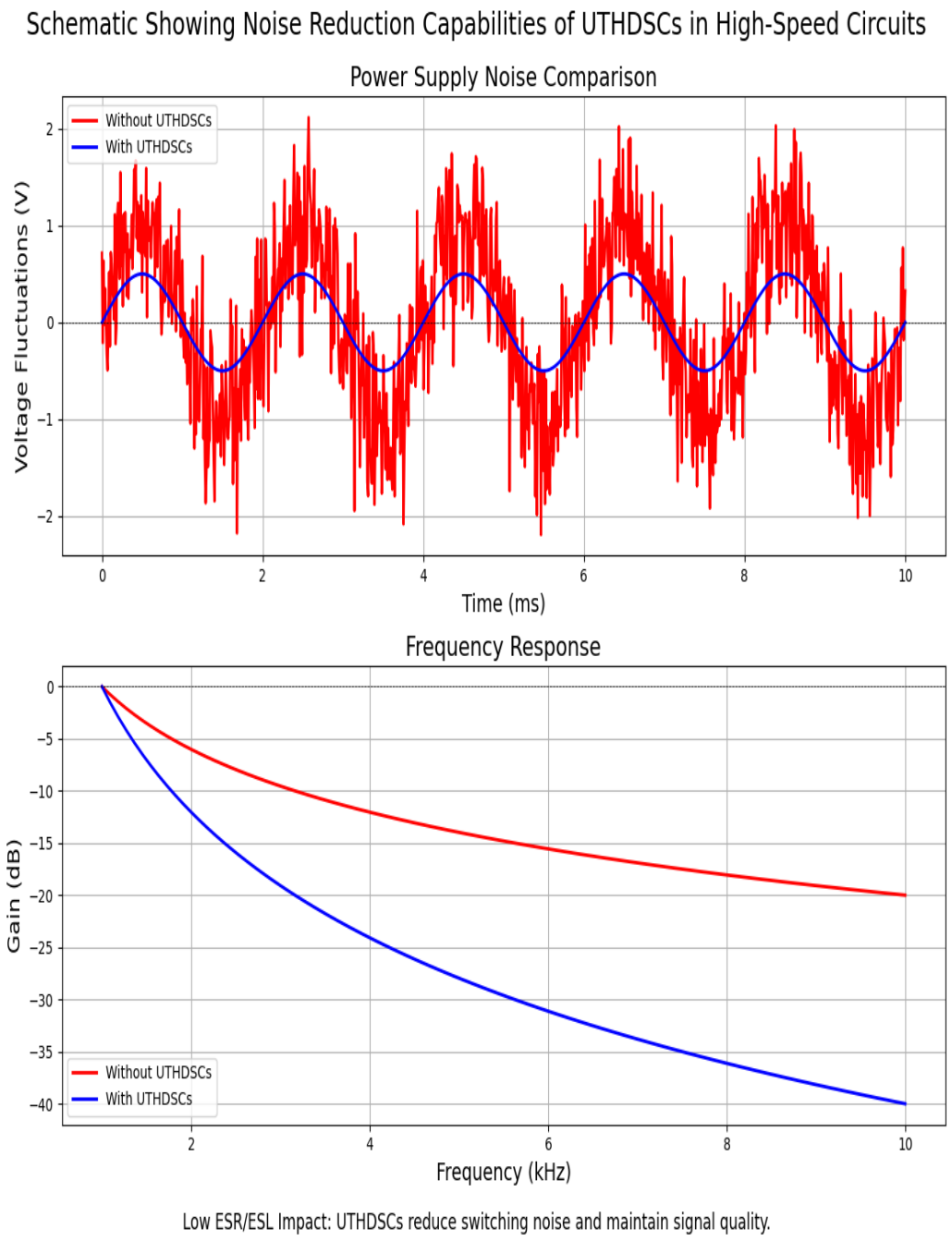
Schematic Showing Noise Reduction Capabilities of UTHDSCs in High-Speed Circuits
Power Supply Noise Comparison
Without UTHDSCs
With UTHDSCs
Voltage Fluctuations (V)
Time (ms)
Frequency Response
Gain (dB)
Without UTHDSCs
With UTHDSCs
Frequency (kHz)
Low ESR/ESL Impact: UTHDSCs reduce switching noise and maintain signal quality.

Figure 2.

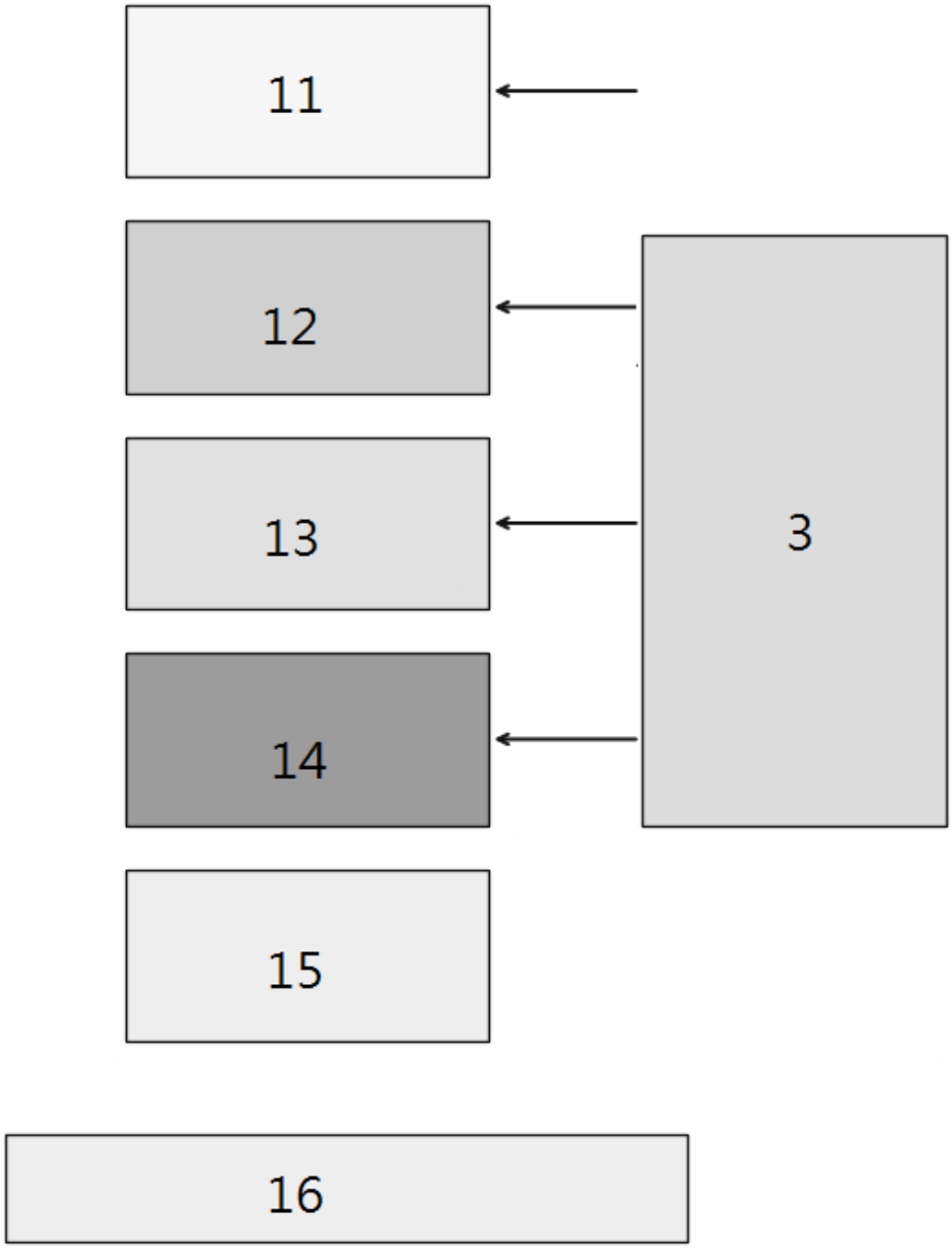

Figure 3.

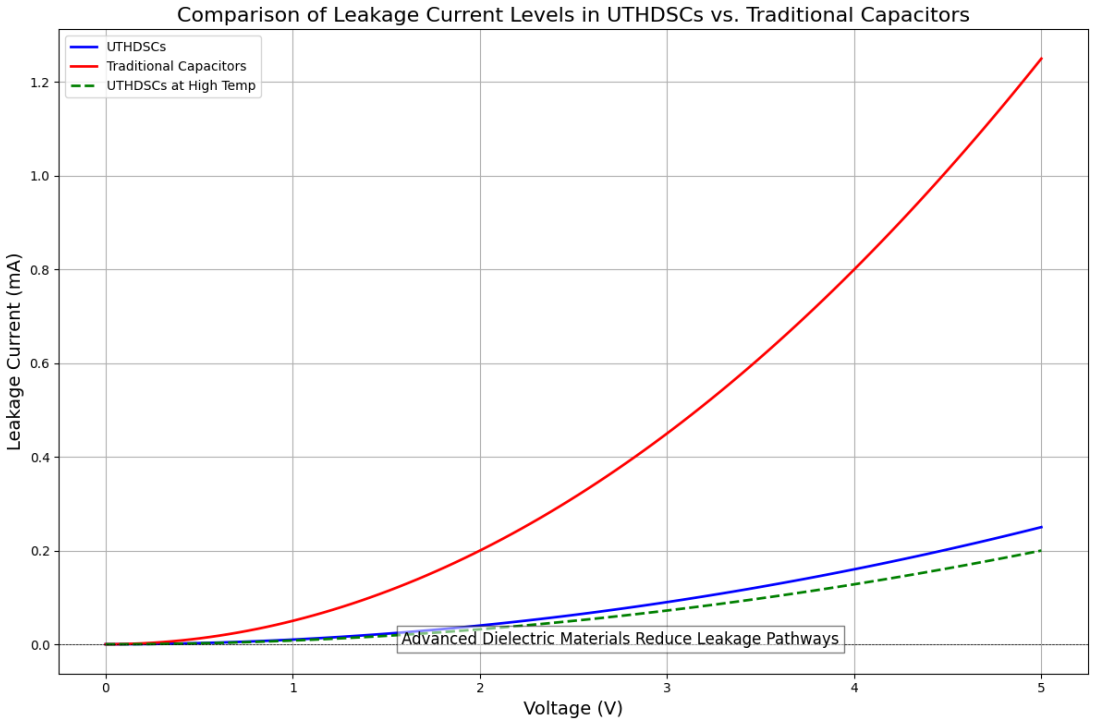

Figure 4.

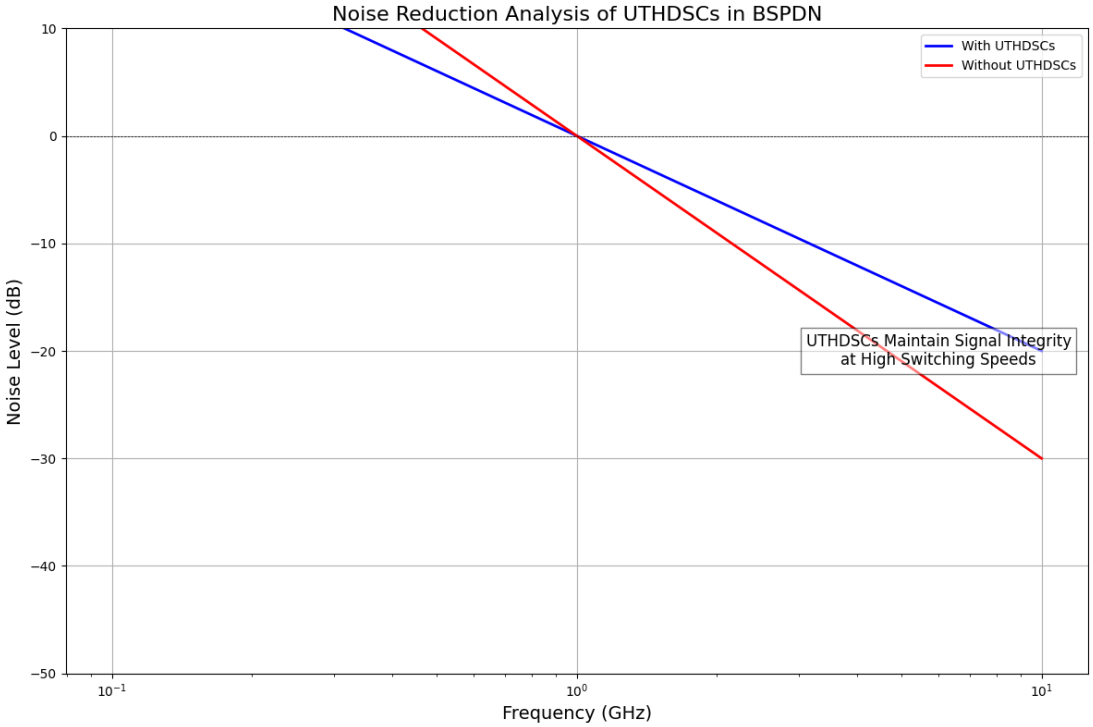

Figure 5.

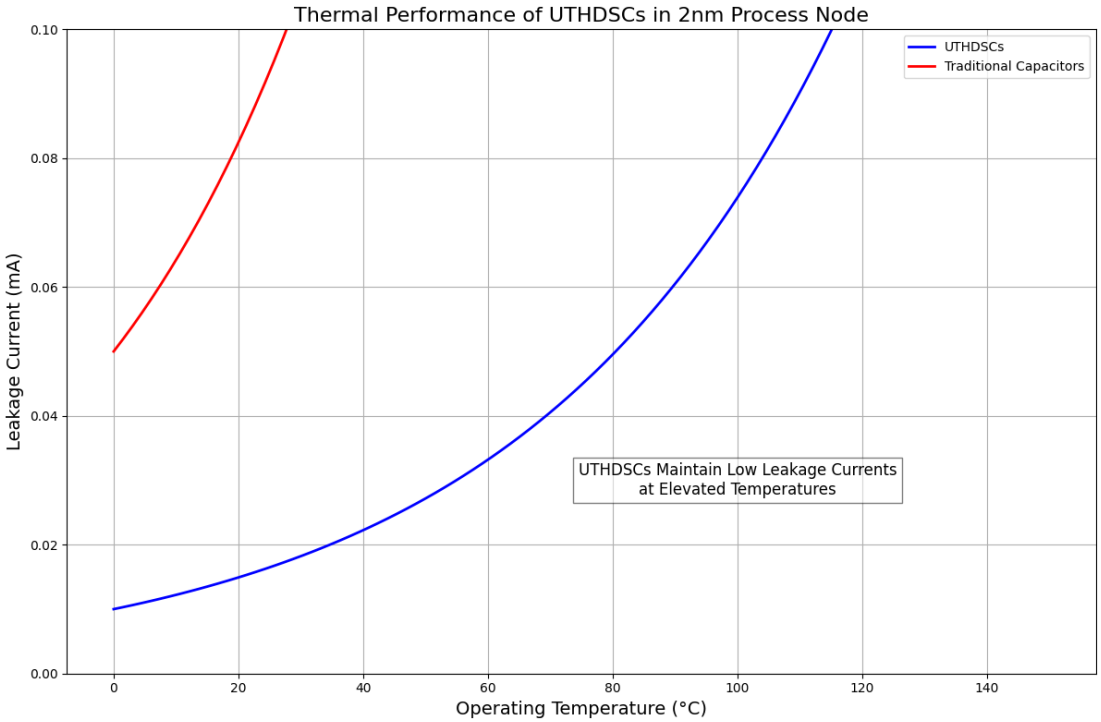

Figure 6.

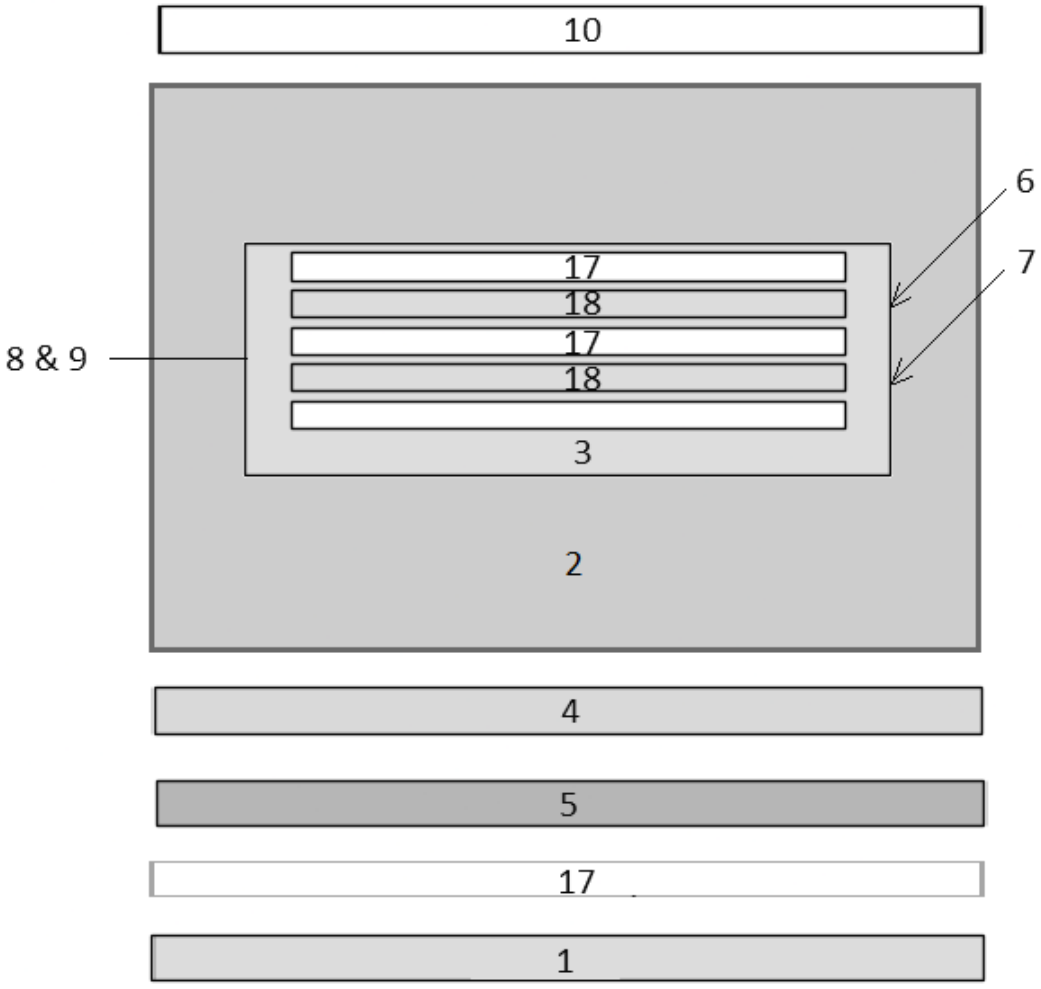

Figure 7.